

FIG. 1

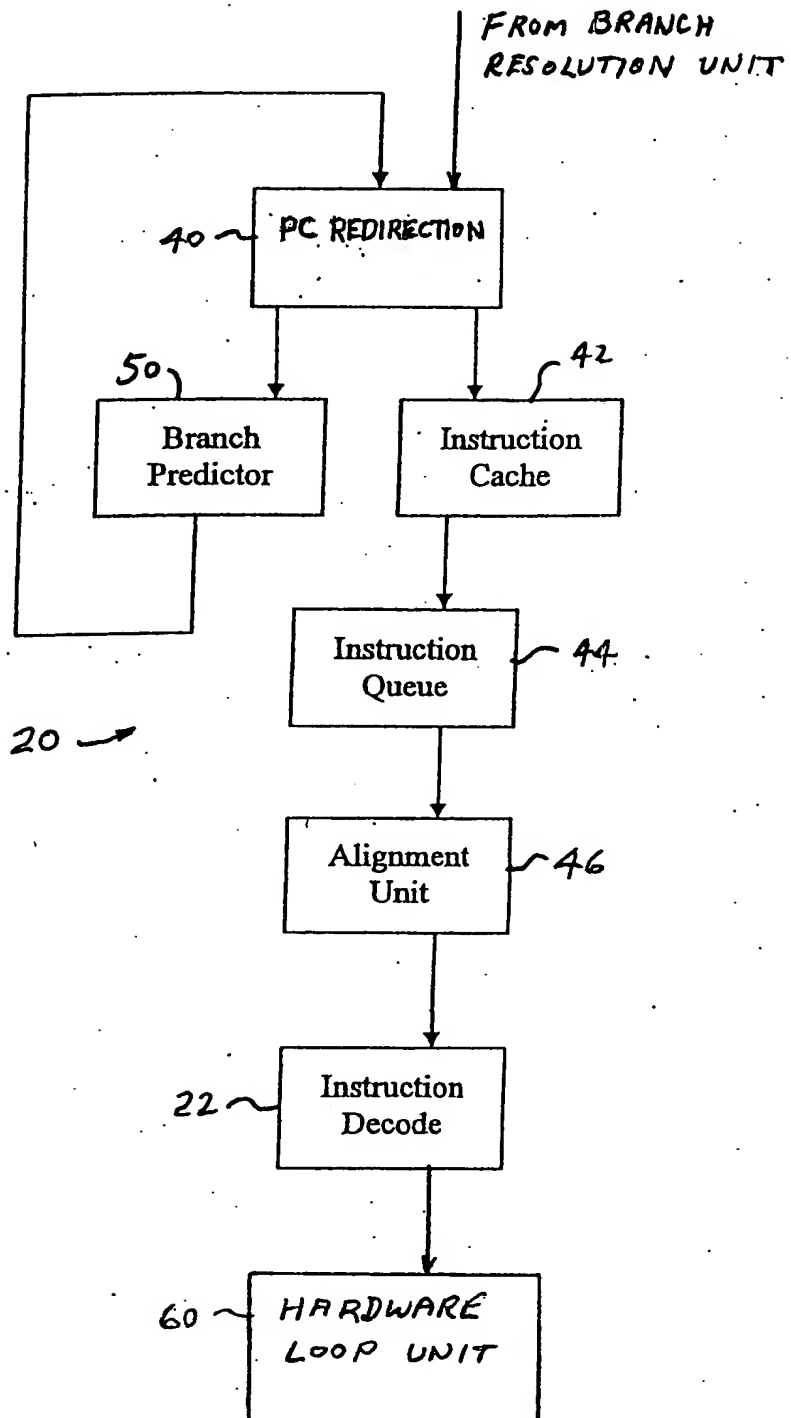


FIG. 2

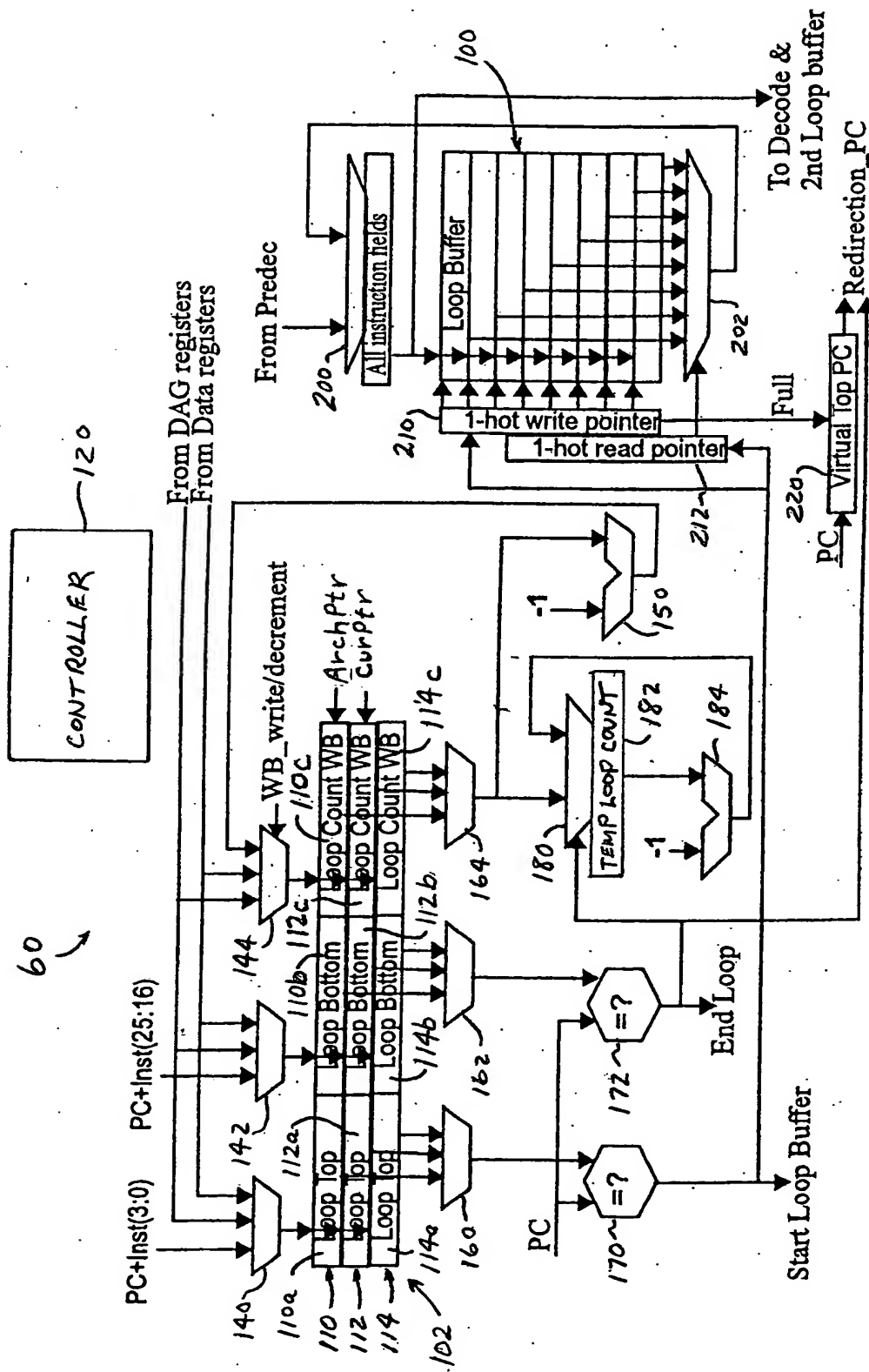


FIG. 3

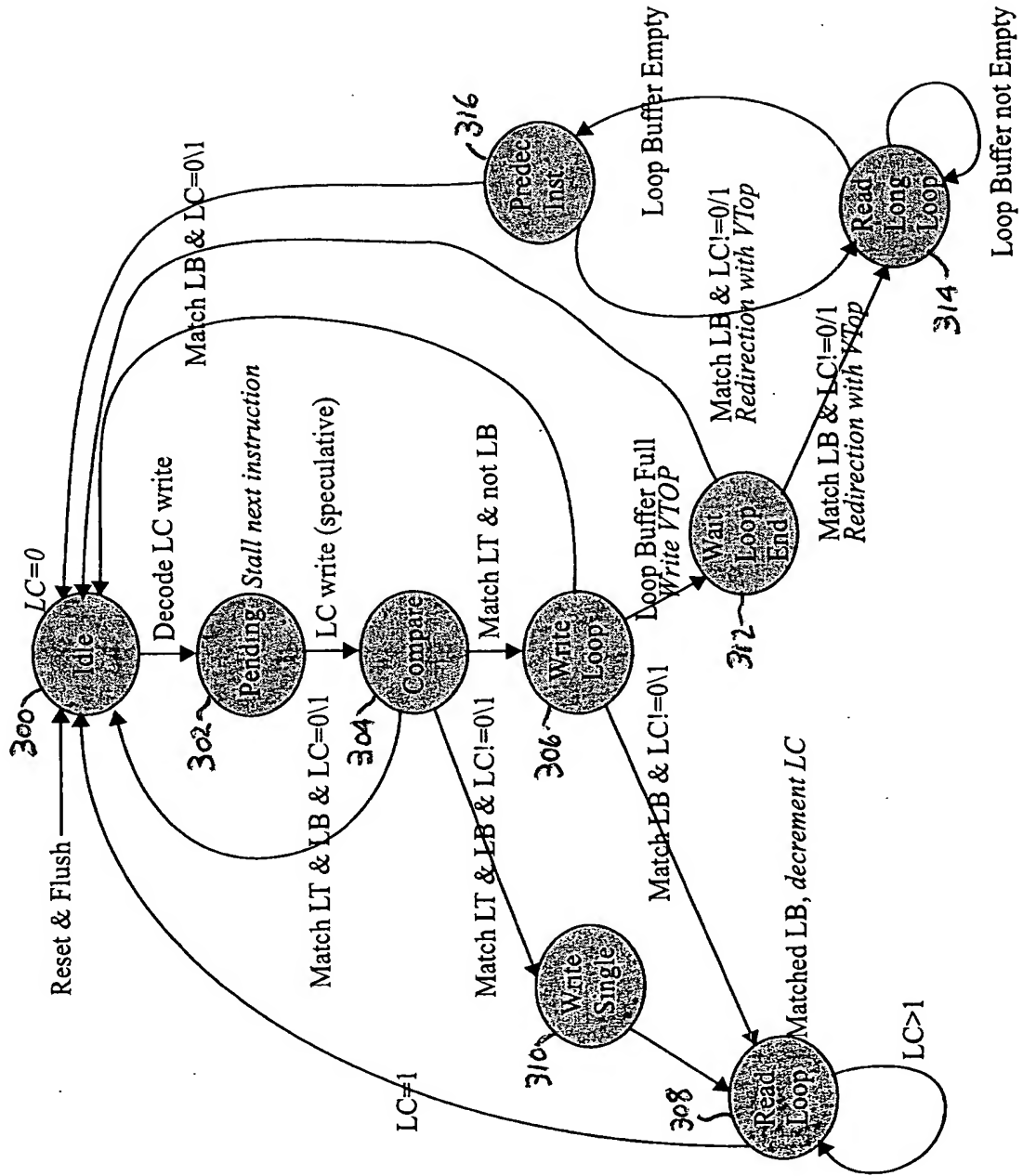


FIG. 4

Inst	PC(7:0)	Inst Length	Offsets	Next PC	Loop Top	Loop Bottom	Loop Count	Loop Buffer	Comment
Lsetup	00110100	32-bit	2/16	00111000	00111000	01010100	Pending	Loopsetup	Loopsetup
I1	00111000	16-bit	-	00111010	Match	-	20	write I1	
I2	00111010	16-bit	-	00111100	-	-	20	write I2	
I3	00111100	16-bit	-	00111110	-	-	20	write I3	
I4	00111110	16-bit	-	01000000	-	-	20	write I,4	
I5	01000000	16-bit	-	01000010	-	-	20	write I5	
I6	01000010	32-bit	-	01000100	-	-	20	write I6	
I7	01001000	32-bit	-	01001100	-	-	20	write I7	
I8	01001100	64-bit	-	01010100	-	-	20	write I8	
I9	01010100	16-bit	-	01010110	-	Match	20	write I9 read I1	set Vtop
I11	00111000	16-bit	-	00111010	Match	-	19	read I2	Fetch I9
I12	00111010	16-bit	-	00111100	-	-	19	read I3	

400 ~
401 ~
402 ~
403 ~
404 ~
405 ~
406 ~
407 ~
408 ~
409 ~
410 ~
411 ~

FIG. 5

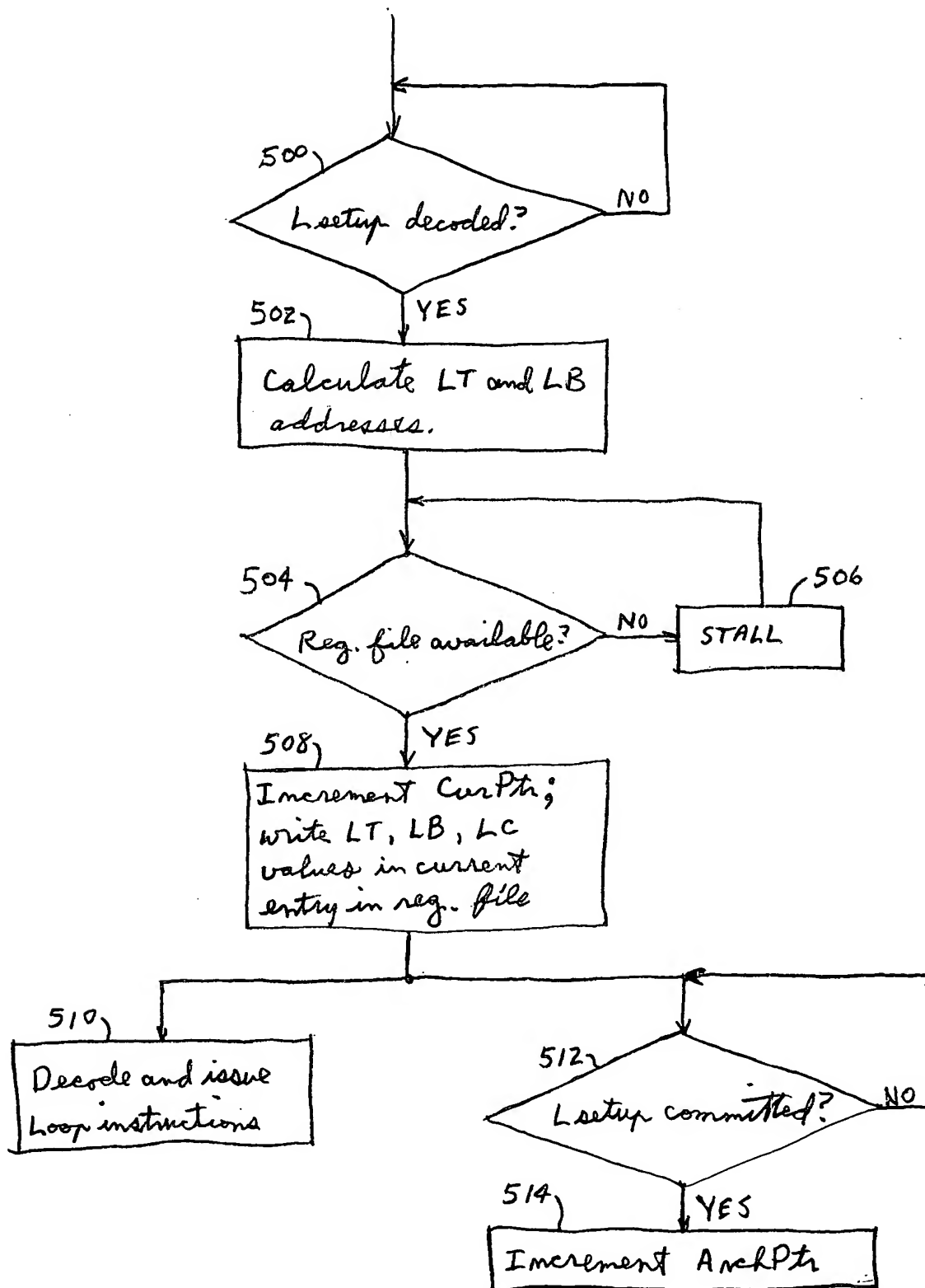
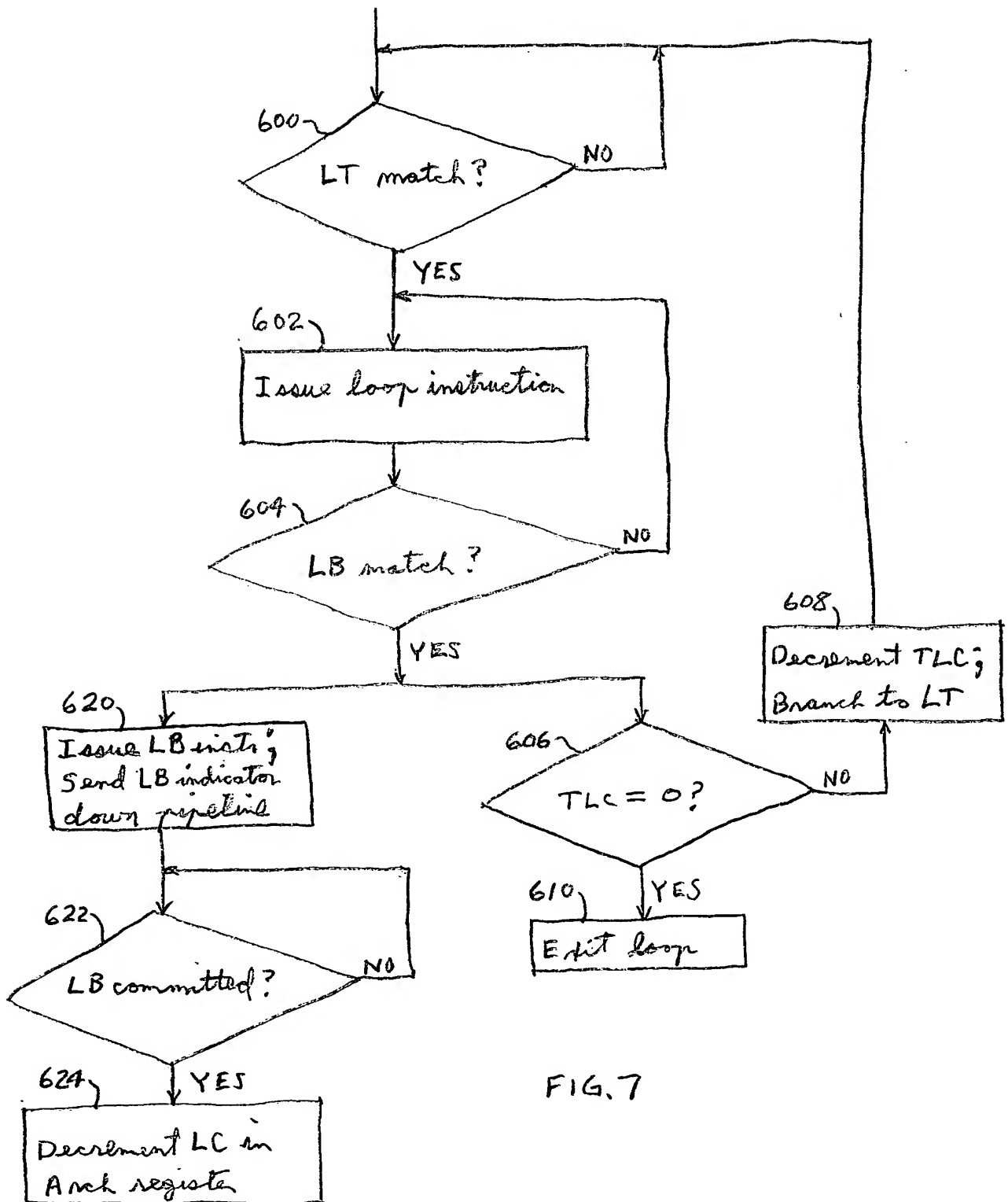


FIG. 6



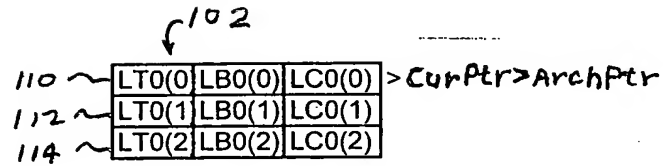


FIG. 8A

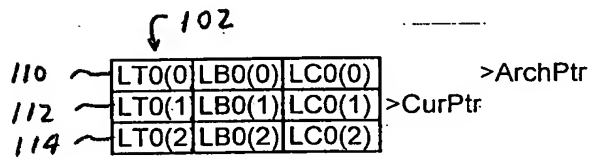


FIG. 8B

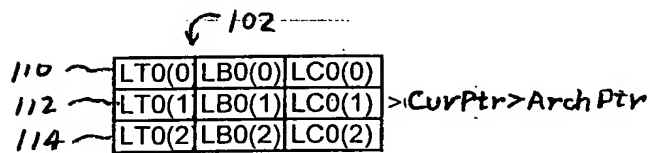


FIG. 8C

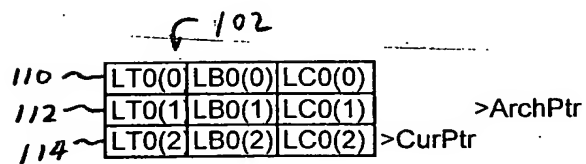


FIG. 8D

Pipe/Cycle	DEC	AC1	AC2	AC3	LS1	LS2	LS3	UC1	LT (o)/LB (o)	LT (i)/LB (i)	LT (i)/LB (i)
701 ~ 1	I1	Loop0							PC+2, PC+6	2,2	
702 ~ 2	I2	I1	Loop0						PC+2, PC+6	1,2	
703 ~ 3	I1	I2	I1	Loop0					PC+2, PC+6	1,2	
704 ~ 4	I2	I1	I2	I1	Loop0				PC+2, PC+6	0,2	
705 ~ 5	Loop1	I2	I1	I2	I1	Loop0			PC+2, PC+6	0,2	
706 ~ 6	I4	Loop1	I2	I1	I2	I1	Loop0		PC+2, PC+6	0,2	PC+2, PC+2
707 ~ 7	I5	I4	Loop1	I2	I1	I2	I1	Loop0	PC+2, PC+6	0,2	PC+2, PC+2
708 ~ 8	Loop2	I5	I4	Loop1	I2	I1	I2	I1	PC+2, PC+6	0,2	PC+2, PC+2
Interrupt 709 ~	I6	Loop	I5	I4	Loop1	I2	I1	I2	PC+2, PC+6	0,2	PC+2, PC+2
710 ~ 10		-	-	-	-	-	-	-	PC+2, PC+6	2,2	-

FIG. 9